JEDEC STANDARD

Test Method for Real-Time Soft Error Rate

JESD89-1B

Addendum No. 1 to JESD89
(Revision of JESD89-1A, October 2007)

JULY 2021

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by
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TEST METHOD FOR REAL-TIME SOFT ERROR RATE

(From JEDEC Board Ballot JCB-20-64, formulated under the cognizance of the JC-14.1 Subcommitee on Reliability Test Metods for Packaged Devices.)

1 Scope

This test is used to determine the Soft Error Rate (SER) of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) for errors which require no more than re-reading or re-writing to correct and as used in terrestrial environments. It simulates the operating condition of the device and is used for qualification, characterization, or reliability monitoring. This test is intended for execution in ambient conditions without the artificial introduction of radiation sources.

JESD89-1 is offered to define concisely the requirements for executing this test in a standardized fashion. It is intended for use in conjunction with JESD89 which includes background on reasons for these requirements.

NOTE 1 Typically, soft error rate characterization by this test method will be executed by the device manufacturer. Other parties may also apply this method appropriately in conjunction with the manufacturer's product data sheet.

NOTE 2 The term real-time soft-error rate (RTSER) is preferred over the term system soft-error rate (SSER).

NOTE 3 Special considerations apply to devices that are more than memory arrays and/or bistable logic elements. These can preclude the application of this test procedure. Refer to JESD89 for further discussion on some examples.

1.1 Applicable documents

JESD89	Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
JESD89-2	Test Method for Alpha Source Accelerated Soft Error Rate
JESD89-3	Test Method for Beam Accelerated Soft Error Rate
JESD22-A108	Temperature, Bias, and Operating Life

2 Apparatus

The performance of this test requires equipment that is capable of providing the particular test conditions to which the test samples will be subjected. (As a practical matter, this equipment will typically provide the means to collect data on many samples under evaluation over the same time period.)

The integrity of the test apparatus shall be verified prior to data collection. The particulars of the verification process are left to the individual investigator for their specific equipment.

2.1 Vehicle design and operation

The circuitry through which the samples shall be biased shall be designed with the following considerations:

The biasing and operating schemes shall consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

The test circuit shall be designed to limit power dissipation such that if a device failure occurs, excessive power cannot be applied to other devices in the sample.

2.2 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under test, (e.g., improper heat dissipation).

2.3 Power supplies and signal sources

Instruments (e.g., oscilloscopes) used to set up and monitor power supplies and signal sources shall be calibrated and have long-term stability. Electrical noise shielding shall be in place to allow for accurate test results.

3 Terms and definitions

absolute maximum rated temperature: The maximum junction or ambient temperature of an operating device as listed in its data sheet and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

absolute maximum rated voltage: The maximum voltage that may be applied to a device and beyond which damage (latent or otherwise) may occur. It is frequently specified by device manufacturers for a specific device and/or technology.

critical charge (Qcrit): The minimum amount of collected charge that will cause a device node to change state and result in a single event upset (SEU).

hard error: An irreversible change in operation that is typically associated with permanent damage to one or more elements of a device or circuit (e.g., gate oxide rupture, destructive latch-up events).

NOTE The error is called “hard” because the data is lost and the circuit or device no longer functions properly, even after power reset and re-initialization.

minimum operating voltage: The minimum power supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet.

3 Terms and definitions (cont'd)

multiple-bit upset (MBU): A multiple-cell upset (MCU) in which two or more of the upsets occur in the same logical word (or frame/column/sector, etc. for FPGAs).

NOTE An MBU is a logical manifestation of a single event.

multiple-cell upset (MCU): A single event that induces several cells (e.g. memory cells or flip-flops) in an IC to flip their state at one time.

NOTE 1 The induced errors are usually, but not always, physically adjacent. This does not imply logical adjacency, since this will depend on how cells are placed and routed (interleaved).

NOTE 2 MCUs can manifest themselves logically as MBUs, multiple SBUs or a combination of the two.

power cycle soft error (PCSE): a single event effect that is not corrected by repeated reading or writing but can be corrected by removal and reapplication of power.

reset soft error (RSE): an SEU that requires re-writing to the device configuration registers in order to return to normal operation without a power cycle operation. This reset can also be considered a reconfiguration (e.g. FPGA) or reprogramming.

real-time soft error rate (RTSER): Soft error rate measurement technique in a naturally occurring alpha particle and neutron environment using a large number of devices to obtain a statistically significant error count. This is in contrast to an accelerated SER test in which an intense radiation source is used on a single, or small number of devices. RTSER error counts can be increased by using a higher neutron flux at higher altitudes, but for the purposes of this specification, the term "accelerated test" is reserved for intense radiation sources that do not occur in natural terrestrial environments. System SER (SSER) is another term that is often used and is considered synonymous with RTSER.

single-event burnout (SEB): An event in which a single energetic-particle strike induces a localized high-current state in a device that results in catastrophic failure.

single-event effect (SEE): An event initiated by a particle strike that causes a transient voltage or current pulse. For various types of SEE, see JESD89B Figure 1.

single-event functional interrupt (SEFI): A single event effect (SEE) that causes the component to reset, lock-up, or otherwise malfunction in a detectable way, but does not result in permanent damage (i.e. hard error).

NOTE A SEFI is often associated with an SBU/MBU in a control bit or register , whereas an SEL is caused by the turn-on of a parasitic thyristor. Many SEFI events can be cleared with a component reset operation (see RSE). In cases where resetting some configuration registers requires a complete power cycle of the device, it can be difficult to distinguish between a SEFI and an SEL. A SEFI event does not nesessarily result in an extended increase in operational current like a high current SEL.

single-event gate rupture (SEGR): An event in which a single energetic-particle strike results in a breakdown and subsequent conducting path through the gate oxide of a MOSFET.

NOTE An SEGR is manifested by an increase in gate leakage current and can result in either the degradation or the complete failure of the device.

3 Terms and definitions (cont'd)

single-event hard error (SHE): A hard error caused by a single event radiation strike.
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single-event latch-up (SEL): An abnormal high-current state in a device caused by the passage of a single energetic particle inducing a parasitic thyristor to turn on and remain in a fixed state regardless of inputs, until the device is power cycled.

NOTE 1. Some SEL events result in a measureable current increase (e.g. latch-up of an IO circuit). Some SEL events may result in a difficult to detect increase in current (micro-SEL) compared to the quiescent current of the entire component (e.g.latch-up of memory cells within a common well).

NOTE 2 A high current SEL may cause permanent damage to the component and result in a hard error. Micro-SEL events are typically non-destructive due to the low current draw and can be cleared by power cycling.

single-event transient (SET): A time dependent radiation induced spurious current or voltage signal on a circuit node. A digital SET (DSET) occurs when an SET in a combinational logic gate (along data or control paths) propagates and is latched to create an error (SEU) in the output of a sequential element. An analog SET (ASET) is a spurious signal in an analog circuit (e.g. a spurious signal on an IO pin, etc.) that causes an erroneous output.

NOTE Not all SETs will result in an upset or soft error. SETs propagating along data and control paths can be masked and never become a latched SEU (logic masking, electrical and temporal masking).

single-event upset (SEU):
An error in a circuit that is not permanent (i.e. not a hard error) caused by a state change of a latch, flop, memory cell or other bistable element from a single energetic particle strike. The energetic strike can occur directly on the circuit element or propagate to that circuit (see SET).

NOTE In many documents and publications, SEU is used to include other soft errors, such as SEFI and SEL.

soft error: An erroneous output signal from a latch or memory cell that can be corrected by performing one or more normal functions of the device (e.g. retrying operation, rewriting data, power cycling, etc.) In many documents and publications, soft error is synonymous with SEU.

NOTE 1 The term refers to an error caused by radiation or electromagnetic noise (e.g. electromagnetic pulse from a nuclear event) and not to an error associated with a physical defect introduced during the manufacturing process. For the purposes of this standard, soft errors are considered to be single particle radiation induced events and not due to other sources, such as signal integrity or noise.

NOTE 2 The terms soft error and soft error rate (SER) have been adopted by the commercial IC industry while other terms, such as SEU, SEFI, etc.. are typically used by the avionics, space, automotive, functional safety and military electronics communities.

NOTE 3 The term "soft error" was first introduced (for DRAMs and ICs) by May and Woods of Intel in their April 1978 paper at the IRPS and the term "single event upset" was introduced by Guenzer, Wolicki and Allas of NRL in their 1979 NSREC paper (SEU of DRAMs by neutrons and protons).

4 Procedure

4.1 Test duration

The test duration shall be specified by internal qualification requirements or the applicable procurement document.

The test duration is defined as the time from the first data write at test conditions to the last read at test conditions. The time spent performing any chamber setup and power down shall not be considered a portion of the total specified test duration.

4.2 Test conditions

4.2.1 Temperature

Unless otherwise specified, the junction temperature for the devices under evaluation shall be controlled to within a tolerance of +/-10°C of each other. (A junction temperature of 40°C is recommended where guidance is needed; other junction temperature conditions may be dictated by customer specification or technical constraints.)

4.2.2 Operating voltage

Unless otherwise specified, the operating voltage shall be the nominal operating voltage specified for the device. In order to characterize SER as a function of Qcrit, a lower/higher voltage is permitted. This voltage shall not exceed the absolute maximum rated voltage for the device and shall be agreed upon by the device manufacturer.

Care shall be taken in all cases to understand what the device operating voltages are in either bypass mode or regulated mode.

4.2.3 Biasing configurations

The parts shall be operated in a dynamic mode during the life test consistent with those described for High Temperature Operating Life (HTOL) in JESD22-A108. Device outputs may be unloaded or loaded to achieve the specified output voltage level. If a device has a thermal shutdown feature, it shall not be biased in a manner that could cause the device to go into thermal shutdown.

4.2.3.1 Real-Time SER test

Unless otherwise stated, the RTSER test shall be configured to provide write/read function to the entire available array of the device samples with insitu pass/fail recording. The cumulative time in each valid data state for each memory array element shall be approximately equal, i.e., a two-state memory element shall see equal cumulative time over the RTSER test in the high state and the low state. It is recommended that the patterns or pattern suite otherwise approximate typical use.

For characterization purposes test conditions can be modified. These include supply voltages, clock frequencies, input signals, etc., which may be operated outside their specified values. When operating outside the application range of the part, predictable and nondestructive behavior of the devices under test shall be assured.

4.3 Test readiness

Prior to running the SER test, a tester readiness check shall be performed. This check shall be performed with the hardware in the manner it will be used for the test. The parts shall be operated to the basic write/read pattern that will be used for the test. The check is completed successfully when no parts fail the basic write/read pattern.

NOTE It might not be possible to obtain a zero error rate due to background terrestrial radiation/alpha particles, but errors due to electrical noise and erratic bits should be reduced below the level of soft errors. If the noise rate is not zero, these errors will be included with the final test results and potentially increase the reported soft error rate.

This check shall be performed before any test in which the test setup was changed.

4.4 Handling

All testing shall follow appropriate procedures for safe handling and ESD control.

5 Measurements

The RTSER test requires that the output of each device be monitored and checked against the expected result in a manner such that the time between reads is less than 0.10 of the mean time between errors. This frequency is intended to help distinguish between multiple errors caused by a single event and multiple errors caused by multiple events.

6 Failure criteria

Any result that does not match expectation is a possible soft error and shall be recorded. If a possible error is identified, action should be taken to verify that it is a soft error.

Care shall be taken to minimize electrically noisy test environments and, thereby, errors related to the equipment and not the device.

Consideration shall be given to discriminating among the error types which can be encountered.

To distinguish a soft error in the device from an error during the system read, the data shall be read more than once at each readout. An error which is not consistently observable through repeated reading shall be considered a “transient” error and is most likely due to noise or device instability (e.g. erratic bit), not a radiation strike. An error which remains uncorrect by additional reading but is corrected by re-writing shall be considered a soft error.

NOTE A noise induced error occurring on the write cycle will remain in memory until it is over-written and appear to be a soft error. Therefore, care should be taken to eliminate these events in design of the test equipment.

6 Failure criteria (cont'd)

To differentiate among soft errors and single-event hard errors (SHE), data shall be rewritten into the device and re-read. If the error is corrected by re-writing, it shall be recorded as a soft error. If the error repeats after re-writing, it is not necessarily a hard error. A reset operation and/or power cycle should be performed to determine if the upset was an SEFI/RSE or SEL, Faults which persist after writing into or re-reading either data state after a power-cycle shall be recorded as hard errors (SHE). (See JESD89 Figure 1 for diagram of terms.)

Any soft error that affects multiple cells in a single read period through the memory array --and that cannot be otherwise demonstrated to be a set of independent cell errors -- shall be reported as a multiple-cell error and classified and counted according to its failure signature. The independence of cell errors can be demonstrated by distinct separation in the time of occurrence, established separation of failing physical addresses, and/or independence of the local array controls and supports for the affected cells.

NOTE An assessment of fault independence based on a distinction of tester timestamps shall consider the delay time between the event and read record. (For example, two errors caused by the same event can have different tester timestamps depending on when they are read within the read cycle of the entire chip and when the event happens within that read cycle.)

Where possible, it is desirable to identify the subset of PCSE that are SEL (as by measurement of anomalous current or bit error count due to latchup in memory cells). Likewise where possible, it is desirable to identify the subset of soft errors that are SEFI. For memory arrays, SEFI may be distinguishable by the extent of related array addresses that are affected (as in an entire array or array subset dependent on operation of a common latch).

7 Report

The following items shall be contained in the final report for any RTSER test:

1. Sample size (number of devices tested)
2. Amount of array or bistable logic elements tested per device
3. Supplier, supplier part number, and die revision (if applicable)
4. Circuit type (e.g., SRAM, DRAM, etc.)
5. ECC description (type and coverage) or "tested per data sheet, ECC unknown"
6. Package description (e.g., connection to chip, materials, geometries) with description of any modifications made for SER testing
7. Test duration
8. Portion of test duration that is cumulative 'dead' (untested) time (Time that is untested between a read followed by a write)
9. Calendar dates and times for data collection
10. Voltage (external supply, use of internal regulated, back bias if applicable)
    NOTE Reporting an internal regulate voltage level is optional, but encouraged where the portability of the date to other devices is of interest.

7 Report (cont'd)

11. Temperature during test (at minimum, ambient temperature; if available, junction temperature as well)
12. Core cycle time or frequency or designation as "static" test (i.e. data written to memory and held for a predetermined time before reading back out) with special notation of cycle times different than product data sheet
13. Refresh rate, where applicable
14. Test pattern(s), including the logical data pattern and, if known, the physical data pattern
15. Tester (commercial model and/or physical description)
16. Test board description
17. Special shielding from radiation sources, if any
18. Stacking or other multi-device configurations used during testing
19. Problems or unusual behavior of the devices during test

    NOTE. If any observed errors are going to be subtracted from the soft error rate calculation, the assumptions and calculation technique should be clearly stated.
20. Soft Error Fail information:
    a. Count of each soft error type (e.g. single cell, multi-cell, SEL, SEFI, etc.)
    b. Calendar date and time of each error
    c. Identification of those soft errors that are multiple-cell errors
    d. Failing logical address or addresses
       NOTE Interpretation of multi-cell errors is enhanced by an understanding of the physical relationship of failing addresses
    e. Test conditions (voltage, ECC usage, data pattern, etc.) where multiple conditions are applied within the same RTSER
    f. Failure rate in test condition. Ideally, the failure rate should should be identified on both a per-bit (or other circuit element) basis as well as a per-event basis. At minimum, the basis for any given failure rate shall be clearly identified.
21. Location of devices under test, including
    a. Latitude and longitude
    b. Altitude
    c. General building description and location within building (e.g., 1 floor below ground level in a 2-story industrial/commercial building of brick construction)
22. Average atmospheric conditions for test period
23. Periodicity of test readouts
24. Angular orientation with respect to ground level during test of the chip active surface (if known) or the packaged device (if the chip active surface orientation is unknown)

If available, it is recommended to document the following information:

A. Dimensions of active area tested
B. Process technology features (e.g., lithographic node, number and type of metal levels, post-metal insulators like polyimide)

Annex A (informative) Differences between JESD89-1B and JESD89-1A

This table briefly describes most of the changes made to entries that appear in this standard, JESD89-1B, compared to its predecessor, JESD89-1A (October 2007). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

SECTION	DESCRIPTION OF CHANGE
3 Terms and definitions	Various definintions have been update to align with JESD89B
4.3 Test readiness	Note added to indicate that zero errors might not be possible due to terrestrial cosmic ray background
6 Failure criteria	Explanation added to help distinguish between 1) errors from noise vs. a radiation strike and 2) soft errors vs. single event hard errors (SHE).
7 Report	Added note that any observed errors subtracted from the soft error rate calculation should be clearly stated in the final report.

Annex A.1 (informative) Differences between JESD89-1A and JESD89-1

This table briefly describes most of the changes made to entries that appear in this standard, JESD89-1A, compared to its predecessor, JESD89-1 (June 2004). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page **Description of change**

At time of publication a change page was not provided.

Standard Improvement Form JEDEC JESD89-1B

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☐ Test method number _____ Clause number _____

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